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EXAMINER

ODLAND, DAVID E

ART UNIT	PAPER NUMBER
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2662

DATE MAILED: 11/13/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/621,031

Applicant(s)

GURA ET AL.

Examiner

David Odland

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-59 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-59 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4,5,7-9.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed on 09/16/200 (paper number 4) fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. Namely, the articles referenced (paper number 4), have not been considered because there is no copy of these references. Note these references are crossed out on the accompanied copy of the IDS.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 27-31 and 44-48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 27 recites "...each of the requesters provides an indication of priority on a bus logically combining the indications of priority..." in lines 1-3. These limitations are confusing; it is unclear who the requesters are providing the priority indications to and how a bus, which is known in the art as merely a transport mechanism, can perform a 'combining' function. Furthermore, it is unclear what is meant by 'logically combining'. Note, claim 44 is also rejected for the same reasons as 27.

Claims 28-31 and 45-48 are rejected because they depend on a rejected claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-6,8-11,25-32,34,35,38-45,47,48,54 and 56-59, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac et al. (USPN 6,370,148), hereafter referred to as Calvignac in view of Davis et al. (USPN 5,835,491), hereafter referred to as Davis.

Referring to claims 1,2,3,5,6,9,10,35,40,56 and 58, Calvignac discloses an arbiter comprising (an arbitration system (see figure 1)) a plurality of requesters (a plurality of input adapters that comprise a plurality of input buffers (see figures 1 and 2)), a plurality of resources coupled to the requesters through a transport mechanism (a plurality of output adapters coupled to the input adapters through a switch matrix (see figure 1)) and wherein a requested resource is responsive to a plurality of requests to selectively grant one of the requests according to requester priorities, the requester priorities being inversely related to a number of requests being made by respective requesters (first, a row is chosen by the arbiter, wherein the corresponding input data is sent to the output adapter and this row is chosen based on the lowest number of requests thus the requesters are prioritized inversely related to the number of requests (see figure 5 and column 6 lines 20-25));

requester priorities are recalculated after a resource is granted (the arbiter continuously arbitrates the communication between the input and output adapters (see figures 1 and 2)).

Calvignac does not disclose that the arbiter is distributed among the resources such that the resources receive the requests, evaluate the requests and grant the resource depending on the associated prioritization, wherein the arbiter performs multiple iterations during one arbitration cycle to allocate resources to requesters. However, Davis discloses a system comprising a distributed arbiter wherein arbiters are distributed among a plurality of output/input resources and perform request evaluation, resource granting and they each operate during an arbitration cycle (multiple iterations in one cycle) (see figure 1 and column 4 line 61 through column 5 line 2)). It would have been obvious to one skilled in the art at the time of the invention to implement the arbiter of Calvignac as a distributed arbiter system, as discussed in Davis, because as Davis points out, in column 4 line 66 through column 5 line 2, such an arbiter can be configured as a linear systolic array which has the advantages of having all communications local and electrical loads not growing with array size, thus enabling linear scaling of the switch. Furthermore, it would have been obvious to combine Calvignac with Davis because doing so would make the system of Calvignac more reliable since if one arbiter was to malfunction the other arbiters can still perform their operations. Note, regarding claims 56 and 58, Calvignac does not disclose that the method is implemented using a computer program. However, it would have been obvious to one skilled in the art at the time of the invention to implement the Calvignac system in software rather than hardware because software based systems are cheaper, in terms of development costs, to implement than hardware and software is also easier to upgrade than hardware.

Referring to claims 4,38,41,42, 57 and 59, Calvignac discloses the system discussed above. Furthermore Calvignac discloses granting at least one of the plurality of resources to a requester according to a round robin scheme, thereby avoiding starvation (a double round robin approach is used to form the request and fairness matrices that are used to arbitrate input to output and prevent starvation by making sure all connections are ultimately made (see column 5 lines 31-67 and column 6 lines 55-60)).

Referring to claims 8 and 11, Calvignac discloses the system discussed above. Calvignac does not disclose that when a resource is granted to a requester the requester removes requests for other resources so that multiple grants are not received during arbitration. However, it would have been obvious to one skilled in the art at the time of the invention to implement such features in Calvignac because doing so would make Calvignac operate more efficiently since one request has been granted and being used by the requester there is no need to keep the requests for the other resources since doing so would waste time and space of the system.

Referring to claims 25 and 26, Calvignac discloses the system discussed above. Furthermore Calvignac discloses that the resources do not transmit grant indications to requesters (the resources are not involved in sending grant information to the requesters (see figures 5 and 6)), each requester determining grant values according to received information from other requesters (the arbiter receives information from other requesters and performs arbitration in order to grant access to one of the requesters (see figures 5 and 6)) and the requesters and resources are synchronized in regards to round robin positions (a round robin arbitration is performed and thus they are synchronized (see figures 5 and 6)).

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Referring to claims 27-31, Calvignac discloses the system discussed above. Furthermore, Calvignac discloses that each of the requesters provides an indication of priority on a bus logically combining the indications of priority, the priority being related to a number of requests being made by each of the requesters (the arbiter gives one of the input adapters priority to use the bus connecting the input adapter to the output adapter (see figure 1));

wherein the indications of priority are unary coded, one bit corresponding to one request (each request is represented by one bit (see figure 3));

wherein the bus logically combines the indications of priority (the switch operates all the busses at the same time according to the priority that is granted (see figures 1-3));

wherein the indications of priority are a number of requests of respective requesters (the number of requests are used to determine priority (see figures 5 and 6 and column 6 lines 20-25)); and

further comprising a requester responding to the priority indication on the bus by not sending a request if the priority indication on the bus indicates a higher priority requester is requesting a resource (the requester who sends the least amount of requests is given priority and thus the other requesters are not granted the same resource as that requester (see figures 3-6 and column 6 lines 20-25)).

Referring to claims 32, 34 and 54, Calvignac discloses the system discussed above. Furthermore, Calvignac discloses that the requesters are nodes of a network coupled to input ports of a network switch (the nodes of a network are inherently connected to the input adapter of the switch (see figure 1) and the resources are output ports of the network switch, multiple ones of the output ports being accessible to more than one of the input ports (the resources are

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output adapters of the switch, wherein the input and output adapters are all interconnected by a switch (see figure 1); and

further comprising recalculating requester priorities after each time a resource is granted to a requester (the arbiter arbitrates the resource allocation on an on-going basis (see figure 1 and columns 3-7)).

Referring to claims 39, Calvignac discloses the system discussed above. Furthermore, Calvignac discloses that the arbitration apparatus is one of distributed arbiter and a centralized arbiter (the arbiter is a centralized arbiter (see figures 1-3)).

Referring to claims 43-45,47 and 48, Calvignac discloses the system discussed above. Furthermore, Calvignac discloses that each requester requesting the requested resource respectively provides a requester priority indication to the requested resource (the arbiter receives state information that includes requesting information from each input adapter and their corresponding queues (see figures 1-3 and column 6));

bus coupled to the requesters and resources, and wherein each of the requesters provides an indication of priority on a bus, the bus logically combining the indications of priority, the priority being inversely related to a number of requests being made by each of the requesters (a bus is coupled between all the input adapters and all the output adapters and all the input adapters and the arbiter (see figure 3), wherein priority over each bus in the switch is given to the requester with the lowest number of requests (see figure 3 and column 6));

wherein the indications of priority are unary coded (the requests are indicated by '0' and '1' bits (see figure 3));

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wherein each requester places a unary encoded number of requests on the bus as the indication of priority (the state information, includes requests are is sent to the arbiter in the for of binary bits (see figure 1-3)); and

wherein a requester with a lower priority than indicated on the bus is responsive to the priority indicated on the bus to not send its request to a resource (the requester with the lowest number of requests is granted access to the switch and its buses and thus the other requesters are not allowed to transmit in that bus until its their turn (see figures 1-6 and column 6)).

6. Claims 12-15,23,24,49,51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac in view of Davis and further in view of Chao et al. (USPN 6,449,283), hereafter referred to as Chao.

Referring to claims 12,14,15,and 49, 51 and 52, Calvignac discloses the system discussed above. Calvignac does not disclose that the requesters receive multiple grants from multiple resources during an arbitration iteration or that the one resource determines which requests to grant and send in parallel with other resources determining which requests to grant. However, Chao discloses a distributed arbitration system wherein multiple grants are sent to an input ports arbiter (see column 16 lines 26-67) and the distributed arbiters perform arbitration at the same time and the grants are sent to the corresponding input port arbiter (see figures 11 and 12). It would have been obvious to one skilled in the art at the time of the invention to send multiple grants to the input adapters of Calvignac, as taught in Chao, because doing so would give Calvignac more choices as to which resources to use, thereby making Calvignac more versatile. Furthermore, having multiple grants would allow Calvignac to pick the resource it needs most

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rather than using a resource that is not needed as quickly, thereby making Calvignac more efficient. Lastly, performing any operations in parallel with other operation will speed up the system, thereby making the Calvignac system operate faster. Note regarding claim 52, Calvignac discloses that a round robin mechanism is used and this mechanism avoids starvation (see column 3, 5 and 6 and figures 1-6))

Referring to claim 13, Calvignac discloses the system discussed above. Calvignac does not disclose that the number of arbitration iterations over multiple arbitration cycles varies dynamically. However, it would have been obvious to one skilled in the art at the time of the invention to vary the number of arbitration cycles in the Calvignac system because doing so would make Calvignac more efficient and flexible since not all arbitrations take the same amount of iterations.

Referring to claims 23 and 24, Calvignac discloses the system discussed above. Calvignac does not disclose that the requester being granted its request sends an accept indication to the resource whose grant it is accepting or that a requester determines which of one or more grants to accept, in parallel with other requesters determining which received grants to accept. However, Chao discloses that each input ports arbiter decides at the same time which one of the multiple grants will be used and then an accept signal is sent back to the output ports arbiter informing the output arbiter of the decision (see column 16 lines 126-67 and figures 11 and 12)). It would have been obvious to one skilled in the art at the time of the invention to implement these features of Chao in the Calvignac system because doing so would allow Calvignac to operate more quickly and efficiently since the decisions are made in parallel and the

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output adapters would know which requesters were using it so it could properly serve that requester.

7. Claims 7,36,37 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac in view of Davis and further in view of Riley et al. (USPN 5,301,279), hereafter referred to as Riley.

Referring to claims 7,36 and 50, Calvignac discloses the system discussed above. Calvignac does not disclose that the resources are considered in an order determined according to resource priority wherein the resource priorities being inversely related to the number of requests made for the respective resource such that the resource priorities are recalculated for each iteration and the requester utilizing a round robin scheme to select from among the plurality of grants. However, Riley discloses an arbitration system wherein resources are given priorities and the requester is granted access to the resource based on the resource priority (a plurality of peripheral devices are each given a priority and the requesting processor is granted the resource based on the resources priority (see column 7)). It would have been obvious to one skilled in the art at the time of the invention to implement the arbitration method of Calvignac with respect to the resources in addition to the requesters because doing so would make Calvignac more efficient since the arbitration is performed in both places.

Referring to claim 37, Calvignac discloses the system discussed above. Furthermore Calvignac discloses granting at least one of the plurality of resources to a requester according to a round robin scheme, thereby avoiding starvation (a double round robin approach is used to form the request and fairness matrices that are used to arbitrate input to output and prevent

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starvation by making sure all connections are ultimately made (see column 5 lines 31-67 and column 6 lines 55-60)).

8. Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac in view of Davis and Chao and further in view of Riley et al. (USPN 5,301,279), hereafter referred to as Riley.

Referring to claims 16-18, 20 and 21, Calvignac discloses the system discussed above. Calvignac does not disclose that the resources are considered in an order determined according to resource priority wherein the resource priorities being inversely related to the number of requests made for the respective resource such that the resource priorities are recalculated for each iteration and the requester utilizing a round robin scheme to select from among the plurality of grants. However, Riley discloses an arbitration system wherein resources are given priorities and the requester is granted access to the resource based on the resource priority (a plurality of peripheral devices are each given a priority and the requesting processor is granted the resource based on the resources priority (see column 7)). It would have been obvious to one skilled in the art at the time of the invention to implement the arbitration method of Calvignac with respect to the resources in addition to the requesters because doing so would make Calvignac more efficient since the arbitration is performed in both places.

Referring to claims 19, Calvignac discloses the system discussed above. Furthermore, Calvignac discloses that requester priorities are recalculated each iteration (the request priorities are calculated in an on-going process (see figures 1-6 and columns 3-6)).

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9. Claims 33 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac in view of Davis and further in view of Rehwald et al. (USPN 4,760,521), hereafter referred to as Rehwald.

Referring to claims 33 and 55, Calvignac discloses the system discussed above. Calvignac does not disclose that the requesters are processors and the resources are memories. However, Rehwald discloses a system wherein an arbiter is used to arbitrate the use of plural memories by plural processors (see figure 1 and abstract). It would have been obvious to one skilled in the art at the time of the invention to implement the arbiter of Calvignac, as taught in the system of Rehwald, because doing so would give the processing system of Calvignac the same benefits as the input/output adapter connection switching has, namely that of fair and efficient resource arbitration, thereby making Calvignac even more fair and efficient.

10. Claim 46, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac in view of Davis and further in view of Clark, II et al. (USPN 6,069,573), hereafter referred to as Clark.

Referring to claim 46, Calvignac discloses the system discussed above. Calvignac does not disclose that the bus implements a wired-NOR of the indications of priority. However, Clark discloses an arbitration system wherein a wired-NOR is used as priority inputs to determine the proper input (see claim 5). It would have been obvious to one skilled in the art at the time of the invention to implement a wired NOR, as taught in Clark, in the Calvignac system because doing so would trigger a one when all of the inputs to the bus are zero thus telling the bus not to

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transmit until a resource is granted, thus preventing erroneous data from be communicated and making the Calvignac more reliable.

11. Claims 22 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac in view of Davis, Chao and Riley and further in view of Arimilli et al. (USPN 6,029,217), hereafter referred to as Arimilli.

Referring to claims 22 and 53, Calvignac discloses the system discussed above. Calvignac does not disclose that the requesters receive multiple grants from multiple resources during an arbitration iteration or that the one resource determines which requests to grant. However, Chao discloses a distributed arbitration system wherein multiple grants are sent to an input ports arbiter (see column 16 lines 26-67) and the grants are sent to the corresponding input port arbiter (see figures 11 and 12). It would have been obvious to one skilled in the art at the time of the invention to send multiple grants to the input adapters of Calvignac, as taught in Chao, because doing so would give Calvignac more choices as to which resources to use, thereby making Calvignac more versatile. Furthermore, having multiple grants would allow Calvignac to pick the resource it needs most rather than using a resource that is not needed as quickly, thereby making Calvignac more efficient. Calvignac also does not disclose that one of the multiple grants is chosen based on a random priority. However, Arimilli discloses an arbitration system wherein a plurality of grants are chose randomly (see column 6 lines 33-59). It would have been obvious to one skilled in the art at the time of the invention to implement a randomized grant selection in the Calvignac system because as Arimilli points out, in column 6

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lines 56-58, such randomization helps to prevent livelocks and deadlocks, thus making Calvignac more reliable.

Conclusion

12. The following prior art, which is made of record and not relied upon, is considered pertinent to applicant's disclosure:

- a. U.S. Patent Number 5,742,594 to Natarajan et al.
- b. U.S. Patent Number 6,473,103 to Bailey et al.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Odland, who can be reached at (703) 305-3231 on Monday – Friday during the hours of 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached at (703) 305-4744. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, who can be reached at (703) 305-4750.

deo

November 10, 2003


JOHN PEZZLO
PRIMARY EXAMINER